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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,128	03/29/2004	Thomas T. Hardt	200311280-1	2179

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
WRIGHT, INGRID D	

ART UNIT	PAPER NUMBER
2835	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,128	HARDT ET AL.	
	Examiner	Art Unit	
	Ingrid Wright	2835	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The examiner of record has considered the information disclosure statement (IDS) submitted on 3/29/04.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over. Roscoe et al. (US 6498731 B1) in view of Wallace et al. (US 6628537 B1).

With respect to claim 1, Roscoe et al. teaches (Fig. 2,9) a memory package comprising a first electronics sub-assembly that comprises a circuit board (210) with at least one memory module socket (208) and at least one controller chip, a first cover portion (264) and a second cover portion (262) and a second cover portion (262) connected to said first cover portion (264) and wherein said first and second cover portions (264,262) are moveable between a closed position wherein said electronics sub-assemblies are nested and a memory controller (22), and a second circuit board

(210) with at least one memory module socket (208) except a second electronics assembly supported by a second cover.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the first electronics assembly on the second cover, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Col., 193 USPQ 8.

Roscoe et al. does not teach a controller chip.

Wallace et al. teaches a controller chips (13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the controller chips as taught by Wallace et al. in the invention of Roscoe et al. in order to provide a controlled circuit or system.

With respect to claim 2, Roscoe et al. teaches (Fig. 2) first and second cover portions (264, 262) further comprises a base surface and wherein when said cover portions (264, 262) are in the closed position, the base surfaces of said cover portions (264, 262) face each other.

With respect to claim 3, Roscoe et al. teaches (Fig. 2) the circuit boards (210) of said first and second electronics sub-assemblies are positioned substantially parallel to and offset from each other. when said first and second cover portions are in the closed position.

With respect to claim 4, Roscoe et al. teaches (Fig. 9) first and second cover portions 264,262 are in the closed position, the memory module sockets 208 mounted to said first circuit board are adjacent to the controller chip mounted to the second circuit board and the memory module sockets mounted to the second circuit board are adjacent to the controller chip of the first circuit board.

With respect to claim 5, Roscoe et al. teaches (Fig. 9) each of said first and second cover portions (264,262) further comprises a base surface and said cover portions (264,262) have an open position wherein the base surfaces of said cover portions (264,262) do not face each other.

With respect to claim 6, Roscoe et al. teaches (Fig. 9) the circuit boards (210) of said first are positioned substantially parallel to and substantially co-planar with each other when said first and second cover portions (264,262) are in the open position.

With respect to claim 7, Roscoe et al. teaches (Fig. 9) a hinge (278) pivotally connecting said first cover portion (264) and said second cover portion (262).

With respect to claim 8, Roscoe et al. teaches (Fig. 9) a latch (282) operable to retain said cover portions (264,262) in the closed position.

With respect to claim 9, Roscoe et al. teaches (Fig. 9) an electrical connector (216) operable to couple said electronic sub-assemblies to a processor- based device.

With respect to claim 10, Roscoe et al. teaches (Fig. 9) an electronic sub-assembly further comprises an electrical connector (216) operable to couple one electronic sub-assembly to a processor-based device.

With respect to claim 11, Roscoe et al. teaches (Fig. 9) a handling aperture (288) in at least one of said cover portions (264).

With respect to claim 12, Roscoe et al. teaches (Fig. 2, 9) the circuit board (210) of said first electronics assembly identical to the circuit board (210) of said second electronics assembly.

With respect to claim 13, Roscoe et al. teaches (Fig. 9) a plurality of memory modules (206) received by the memory module sockets.

With respect to claim 14, Roscoe et al. teaches (Fig. 1) a processor (22), a chassis supporting said processor and a memory package comprising, an electronics assembly comprising first and second circuit boards (210), wherein each circuit board is coupled to at least one memory module (206), and a housing assembly supporting said electronics assembly, wherein said housing assembly has a first cover portion (264) supporting the first circuit board and a second cover portion supporting the second circuit board; wherein said memory package has a closed position and an open position, wherein in the closed position said housing engages said chassis (248) and said electronics assembly electrically couples with said processor (22).

Roscoe et al. does not teach at least one memory controller.

Wallace et al. teaches controller chips (13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the controller chips as taught by Wallace et al. in the invention of Roscoe et al. in order to provide a controlled circuit or system.

With respect to claim 15, Roscoe et al. teaches (Fig. 2,9) the first and second circuit boards (210) are positioned substantially parallel to and offset from each other when said memory package is in the closed position.

With respect to claim 16, Roscoe et al. teaches when memory package is in the closed position, the memory modules (206) mounted to said first circuit board (210) are adjacent to the memory controller mounted to the second circuit board and the memory modules mounted to the second circuit board are adjacent to the memory controller mounted to the first circuit board.

With respect to claim 17, Roscoe et al. teaches memory package has an open position wherein said housing is disengaged from said chassis and said electronics assembly is decoupled from said processor.

With respect to claim 18, Roscoe et el. teaches the first and second circuit boards (210) are positioned substantially parallel to and substantially co-planar with each other when said memory package is in the closed position.

With respect to claim 19, Roscoe et al. teaches the electronics assembly further comprises at least one electrical connector (214) coupled to the first and second circuit boards, wherein the at least one electrical connector (214) couples the electronics assembly to said processor.

With respect to claim 20, Roscoe et al. teaches (Fig. 9) the housing assembly further comprises a hinge (278) pivotally connecting the first cover portion and the second cover portion.

With respect to claim 21, Roscoe et al. teaches (Fig. 9) the housing assembly further comprises a latch (282) operable to retain said cover portions in the closed position.

With respect to claim 22, Roscoe et al. teaches (Fig. 9) memory package comprising means for housing a first and second electronics sub-assemblies, wherein each sub-assembly has at least one memory module (206) and at least one memory controller chip mounted thereto', means for moving at least a portion of said means for housing between an open position allowing access to the memory modules and a closed position where the Mo electronics sub-assemblies are nested together.

With respect to claim 23, Roscoe et al. teaches (Fig. 9) means for coupling the first and second electronics sub-assemblies to a processor-based device when said means (260) for housing is in the closed position.

With respect to claim 24, Roscoe et al. teaches (Fig. 9) means for retaining said means (282,284) for housing in the closed position.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Ali et al. US 6188576 B1 & Franke US 6867972 B2 show the state of the art regarding memory packages and assemblies.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ingrid Wright whose telephone number is (571) 272-8392. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn Feild can be reached on (571) 272-2800, ext 35. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IDW

LYNN FEILD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800